UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/672,367	09/28/2000	Francis X. McKeen	042390.P9578	7649

7590 10/04/2007

Blakely Sokoloff Taylor & Zafman
12400 Wilshire Blvd
7th Floor
Los Angeles, CA 90025-1026

EXAMINER	
KIM, JUNG W	

ART UNIT	PAPER NUMBER
2132	

MAIL DATE	DELIVERY MODE
10/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/672,367	MCKEEN ET AL.	
	Examiner	Art Unit	
	Jung Kim	2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,14-16 and 19-22* is/are rejected.

7)☒ Claim(s) *10,11,17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is in response to the supplemental response filed on 8/10/07.

2. Claims 1-12 and 14-22 are pending.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/10/07 has been entered.

Response to Arguments

4. On pg. 6 of the amendment filed on 8/10/07, applicant alleges that "England is merely a software system ... England does not disclose the design of a processor" and hence does not disclose the limitations of the amended independent claims. However, contrary to applicant's allegations, England, in fact, discloses the design of a processor. Col. 6:13-19; fig. 3. In particular, England discloses a bus transaction between a graphics device and an MCH caused by a processor signal. (6:13-65; 12:58-13:49) Moreover, England discloses a processor that uses a processor signal to cause the graphics device to send a bus transaction to the MCH and to enable access to output

data stored in an isolated output area. (6:33-65) As such, England anticipates the amended claims.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by England et al. USPN 6,775,779 (hereinafter England).

7. As per claims 1-9, England discloses a platform comprising:

a. a system memory to store output data in an isolated output area, and a non-isolated area; (col. 5:55-6:12; Rings A-D)

b. a memory controller hub (MCH) coupled to the system memory; (Fig. 1, reference nos. 121, 131 and 133; 6:16-18) and

c. a processor coupled to the MCH to generate a signal to the MCH, the signal indicating whether the output data is to be stored in the isolated output area or the non-isolated area, the signal generated by the processor to further cause the MCH to receive a bus transaction from a graphics device to enable

access to the output data stored in the isolated output area in response to an indication of the signal that the output data is to be stored in the isolated output area of the system memory (2:66-3:17; 6:16-24; 7:50-65; 12:58-13:49, "frame buffer");

d. wherein the bus transaction from the graphics device indicates an isolated transaction;

e. wherein the MCH coupled between the system memory, the processor, and the graphics device, the MCH to permit the graphics device to access the isolated output area only when the graphics devices asserts an isolated access mode (fig. 1, reference nos. 121, 130-132, 140, 141 and 171; fig. 3; 6:19-7:3);

f. wherein the graphics device comprises: a direct memory access controller and wherein local storage of the data in the graphics card from the isolated output area is not permitted; (7:50-55; 13:37-59)

g. wherein only the graphics device is permitted to read the isolated output area; (10:49-57; 12:57-13:18)

h. an operating system nub having a driver to write display data into the isolated output area when the processor is executing in the isolated execution mode; (5:13-35)

i. a link between the graphics device and the MCH having an isolated transaction type (6:19-32; 12:25-13:15);

j. wherein the MCH only permits the O/S nub to write to the isolated output area (12:25-13:15);

k. wherein the link is a secure accelerated graphics port bus (4:15-40);

8. As per claims 12 and 14-16, England discloses a method comprising:

l. establishing an isolated execution environment having an isolated execution mode by a processor generating a signal indicating whether output data is to be stored in an isolated output area or a non-isolated area of a system memory, the signal generated by the processor further causing a memory controller hub (MCH) to receive a bus transaction from a graphics device to enable access to the output data stored in the isolated output area in response to an indication of the signal that the output data is to be stored in the isolated output area of the system memory (col. 5:55-6:12; Rings A-D; Fig. 1, reference nos. 121 and 133; 2:66-3:17; 6:16-24; 7:57-65; 12:58-13:49, "frame buffer"); and

m. Prevent access to output data in the isolated output area of the system memory by any requestor not operating in the isolated execution mode; (6:33-65; 12:25-13:50)

n. Issuing an isolated direct memory access request for display data in the isolated output area from the graphics device (12:25-67); and refreshing the display based on the display data (13:1-14);

o. Identifying if an isolated attribute is present in a request for access to the isolated output area; and denying the request if no isolated attribute is present (6:33-65; 7:50-56; 12:25-13:50);

p. Loading data from the isolated output area into a bit plane on the graphics device; and denying all external access to the bit plane. (6:33-65; 7:50-56; 8:25-32; 12:25-13:50)

9. As per claims 19-22, England discloses an apparatus comprising:

q. A processor to generate a signal to a memory controller hub (MCH), the signal indicating whether output data is to be stored in the isolated output area or a non-isolated area of a system memory, the signal generated by the processor to further cause the MCH to receive a bus transaction from a graphics device to enable access to the output data stored in the isolated output area in response to an indication of the signal that the output data is to be stored in the isolated output area of the system memory (Fig. 1, reference nos. 121 and 133; 2:66-3:17; 6:16-24; 7:57-65; 12:58-13:49, "frame buffer");

r. Wherein the bus transaction is issued through a secure accelerated graphics port (4:15-40);

s. Wherein the bus transaction is issued by a direct memory access controller of the graphics device, the DMA controller to attach an isolated attribute to any isolated output area access request; (6:19-65; 7:50-56; 13:37-49)

t. Wherein the signal generated by the processor has an isolated attribute to indicate execution in an isolated execution mode. (6:33-65)

Allowable Subject Matter

10. Claims 10, 11, 17 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Communications Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung W. Kim whose telephone number is 571-272-3804. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on 571-272-3799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jung W Kim
Examiner